

1 / 14

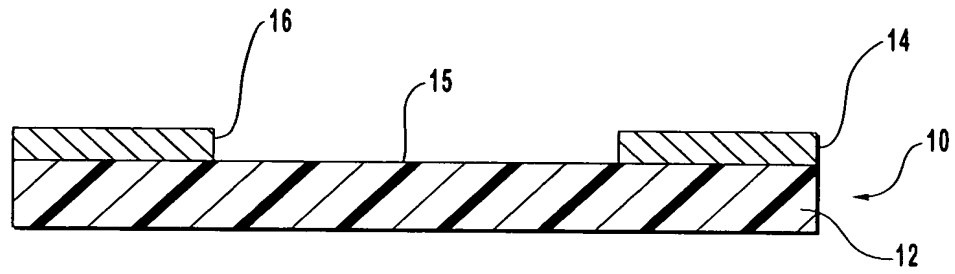


FIG. 1

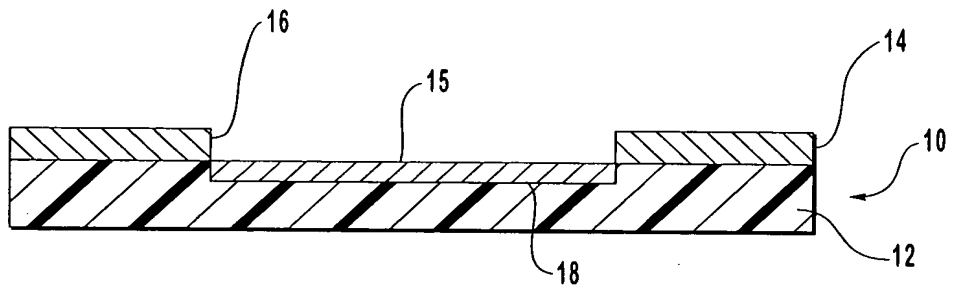


FIG. 2

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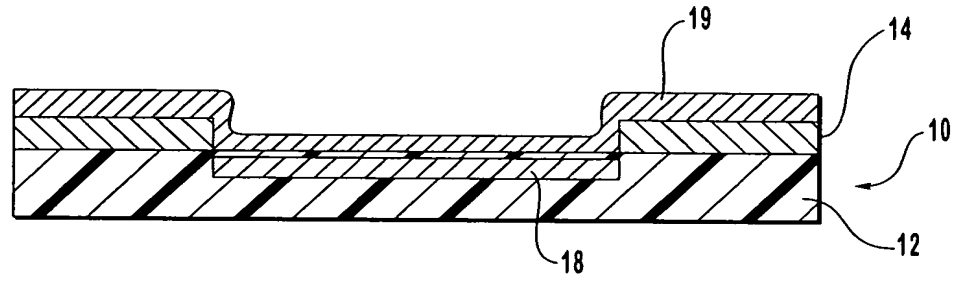


FIG. 2A

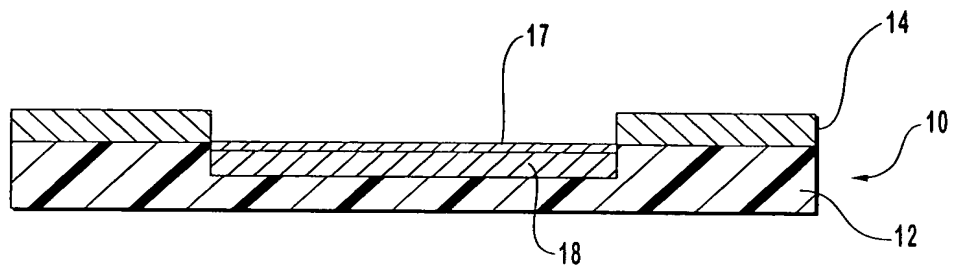


FIG. 2B

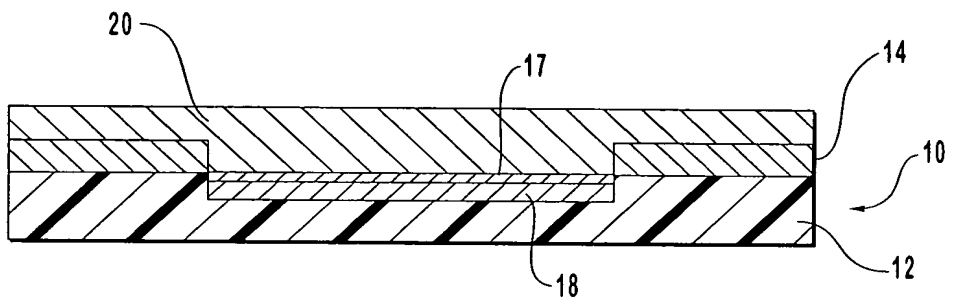


FIG. 3

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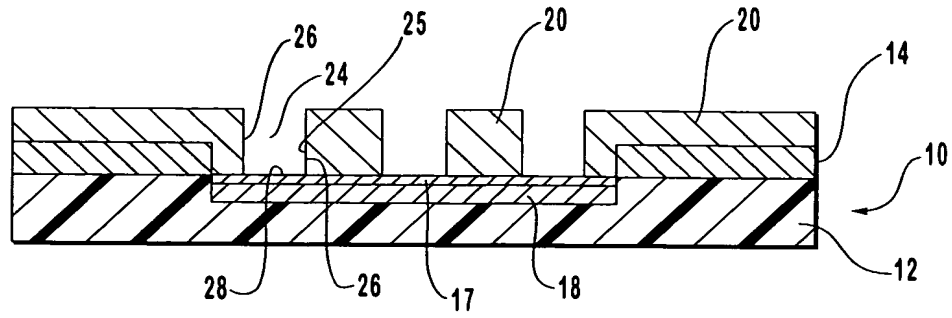


FIG. 4

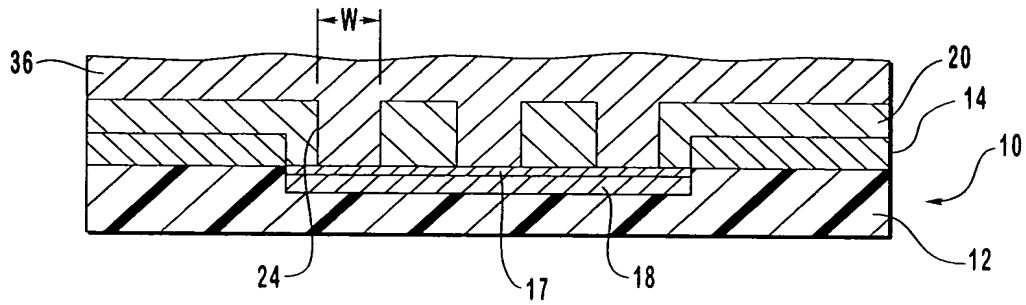


FIG. 5

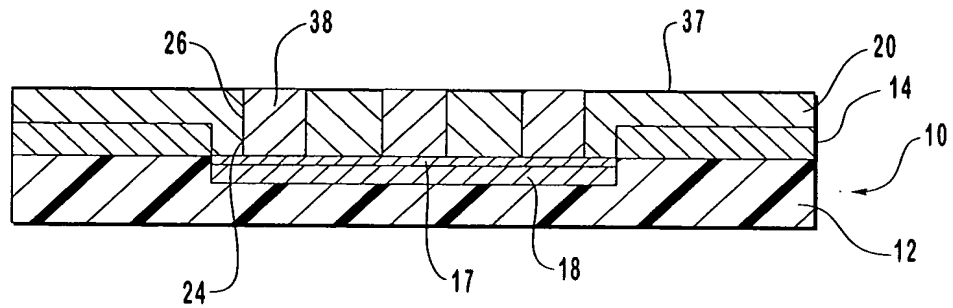


FIG. 6

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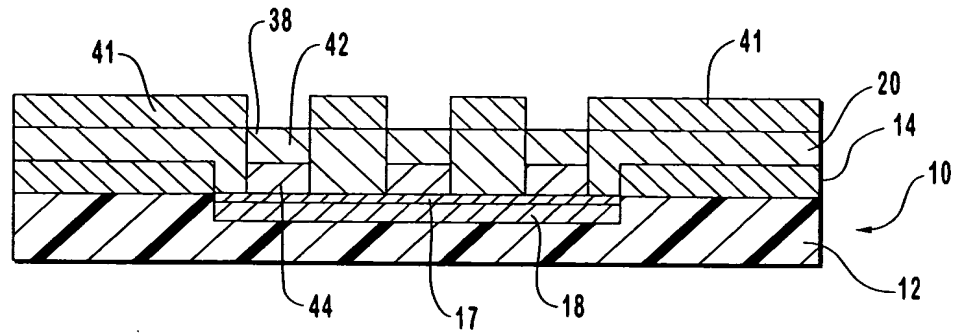


FIG. 7

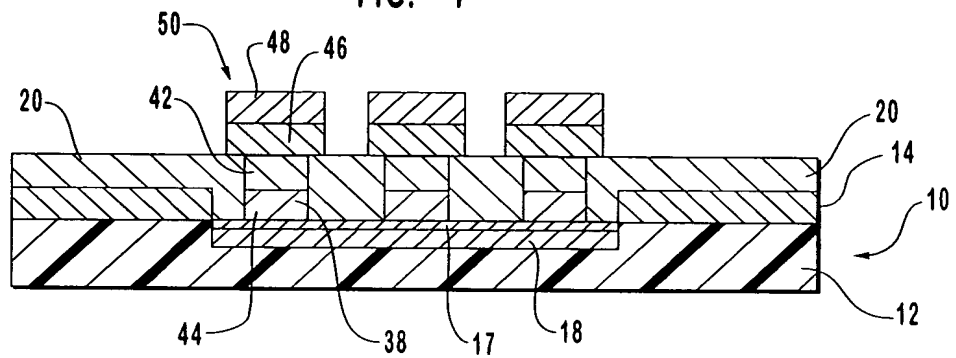


FIG. 8

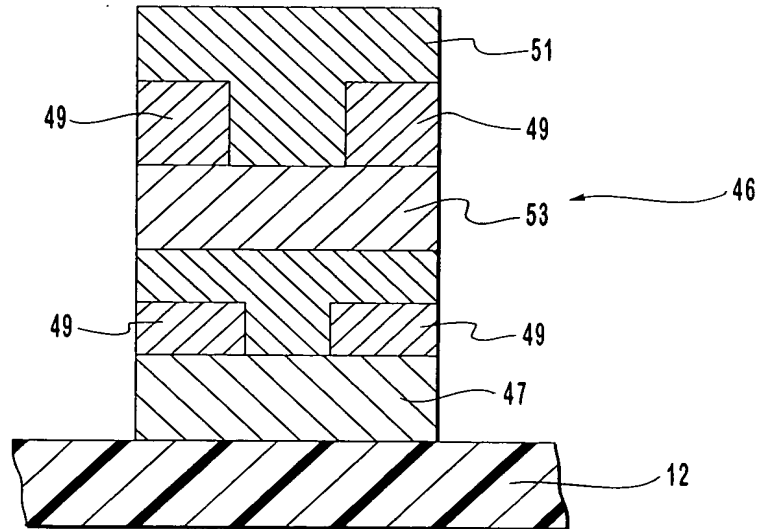


FIG. 8A

FIG. 11

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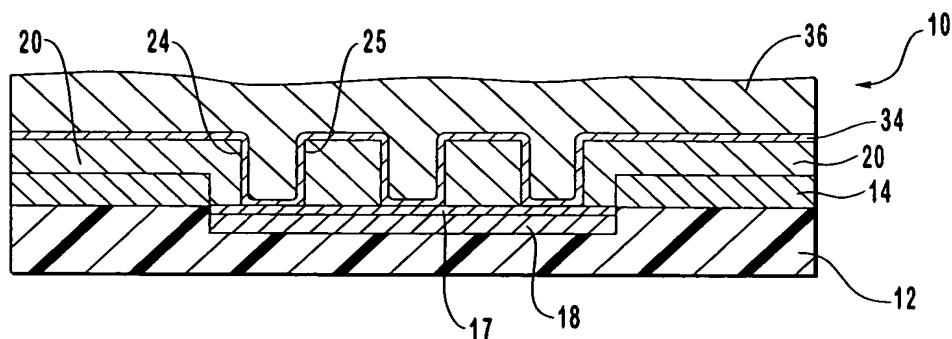


FIG. 12

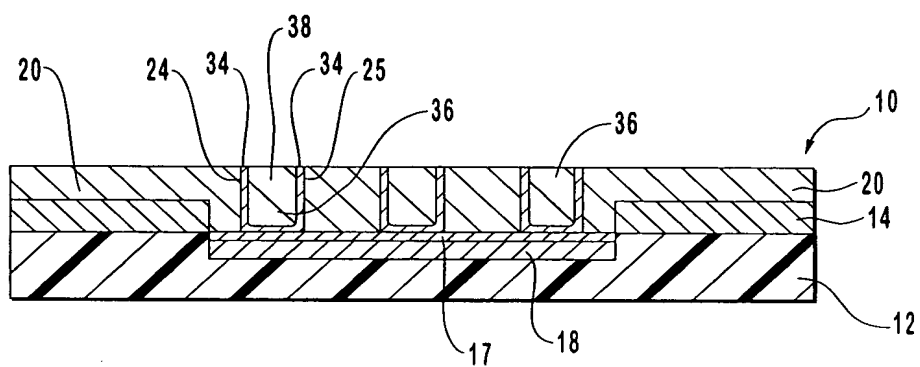


FIG. 13

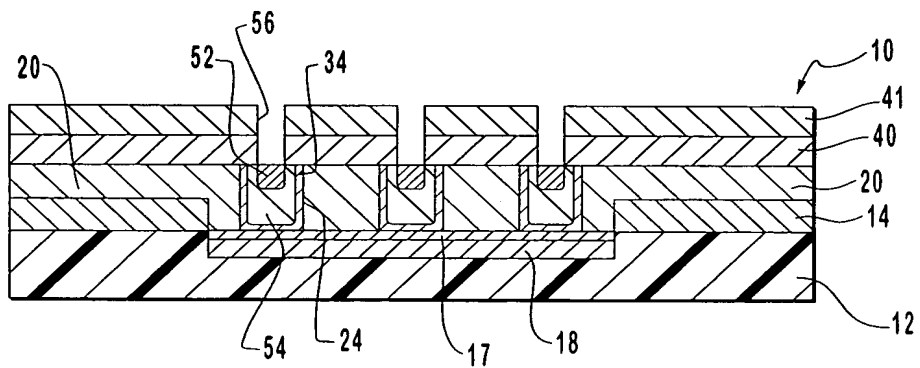


FIG. 14

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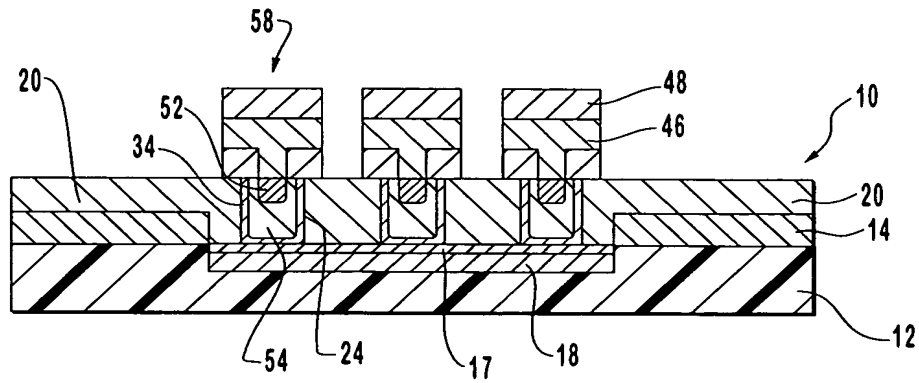


FIG. 15

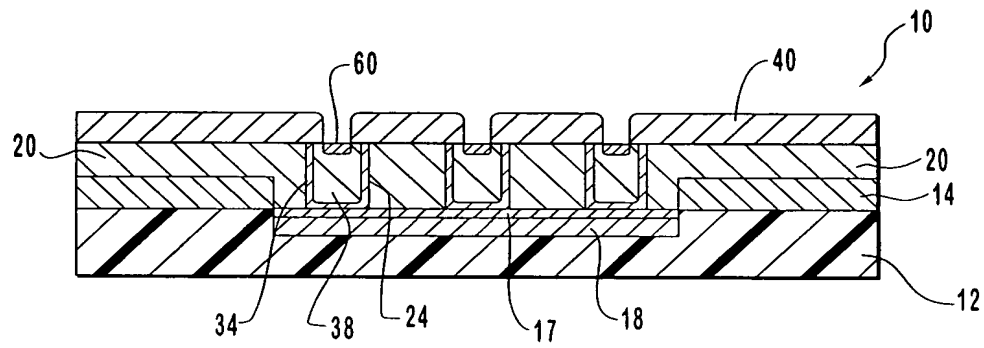


FIG. 16

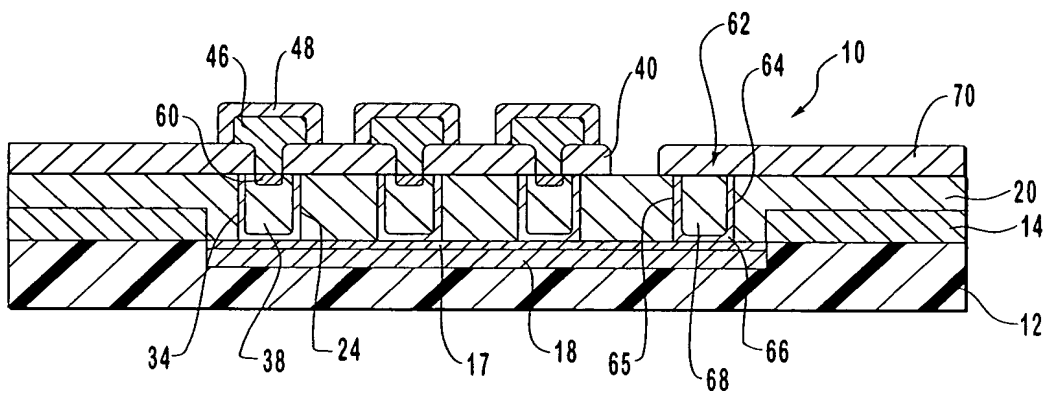


FIG. 17

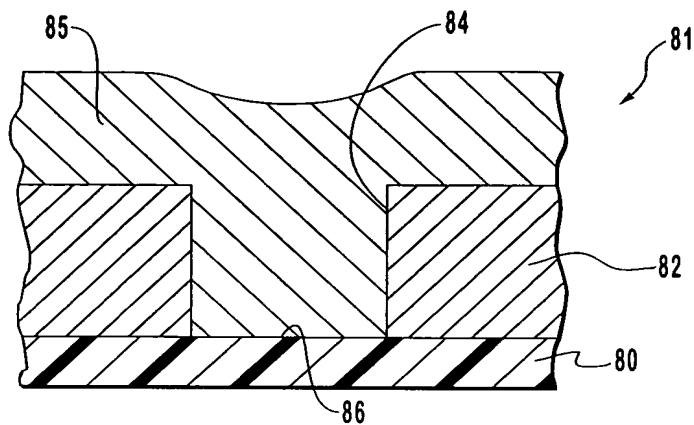


FIG. 18

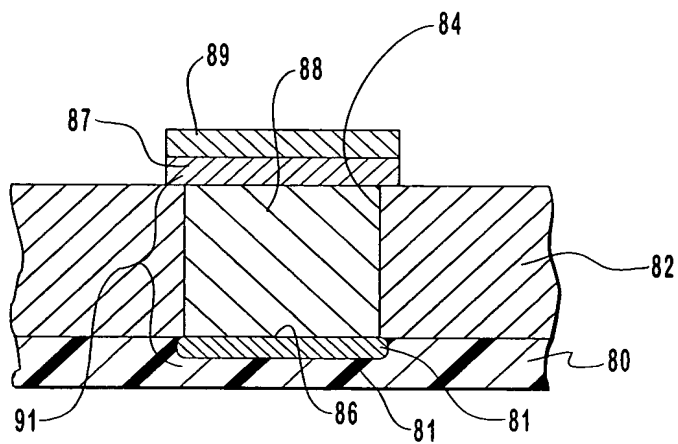


FIG. 19



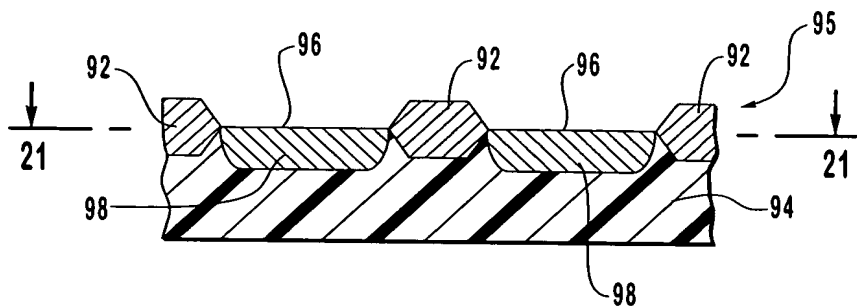


FIG. 20

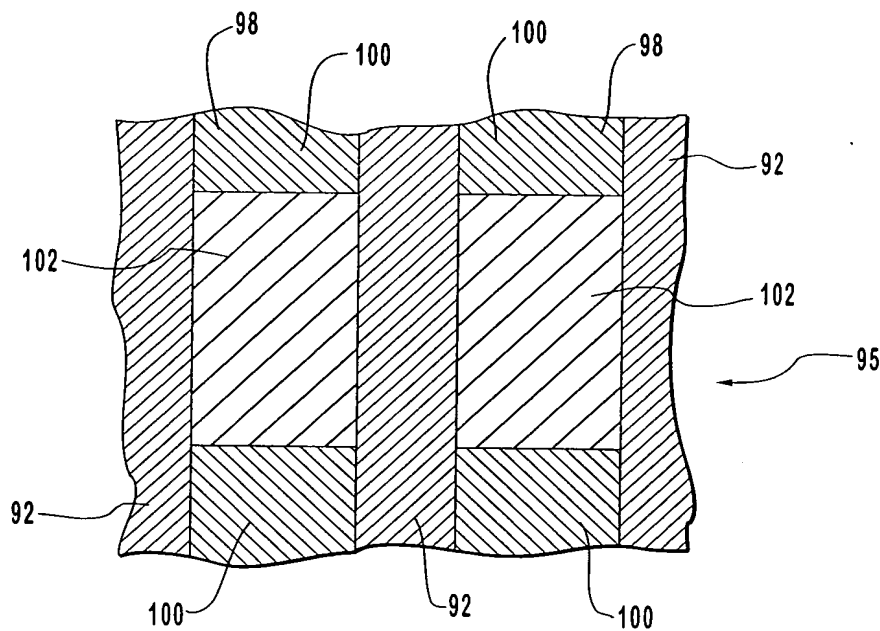


FIG. 21

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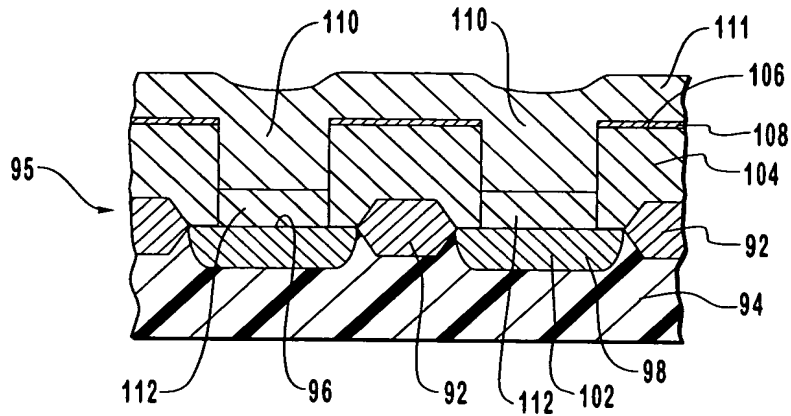


FIG. 22

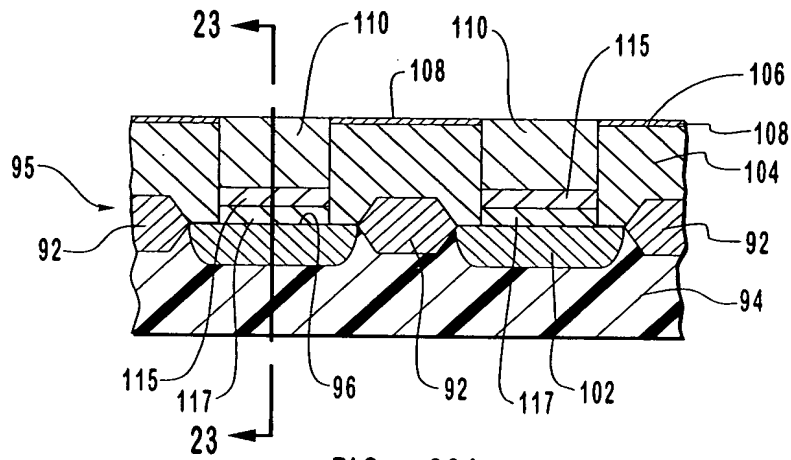


FIG. 22A

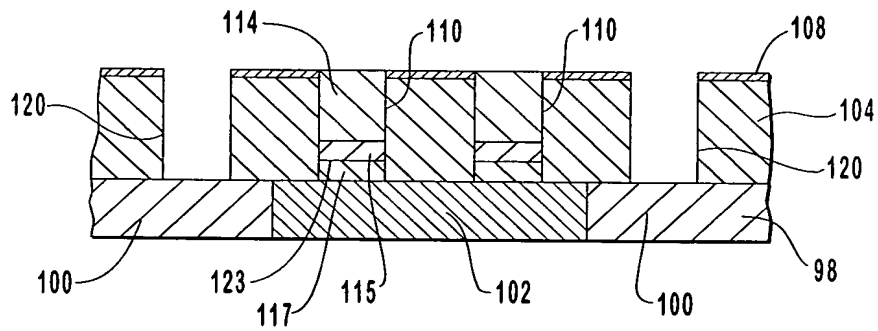


FIG. 23

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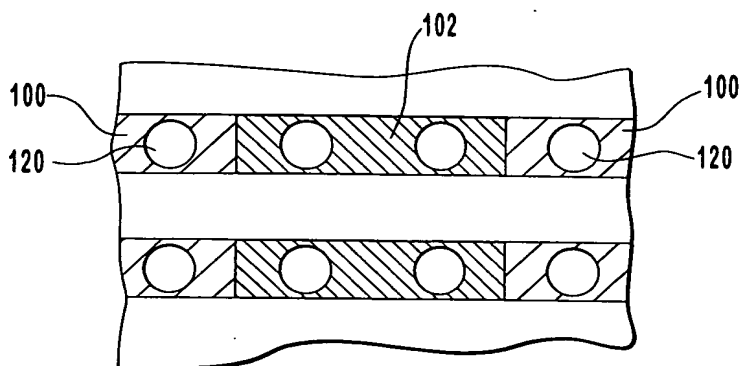


FIG. 24

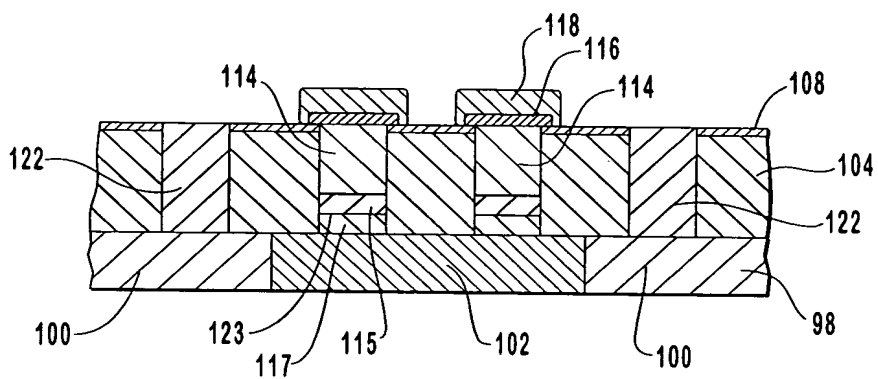


FIG. 25

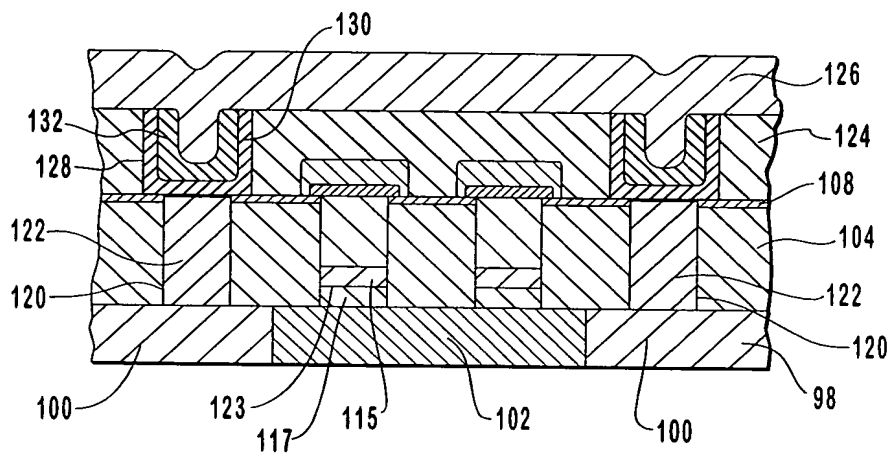


FIG. 25A

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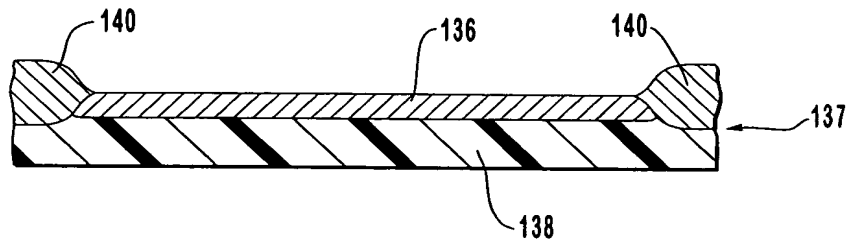


FIG. 26

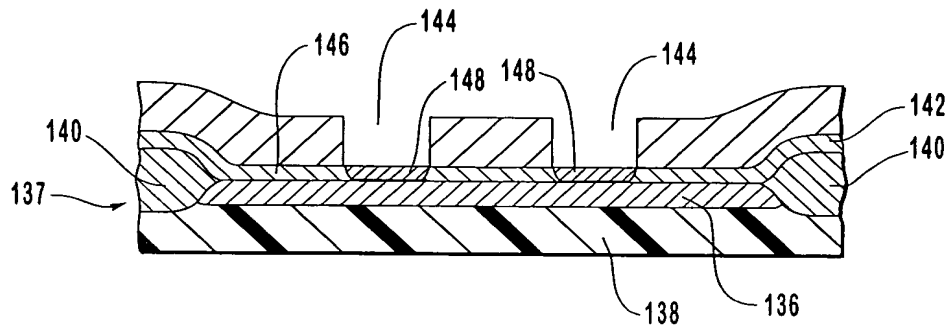


FIG. 27

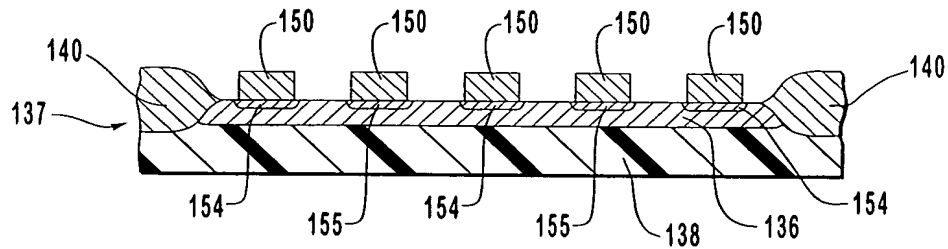


FIG. 28

A cross-sectional view of a semiconductor device. The device consists of a substrate 137 with a bottom layer 152. A grid of pillars is formed on the substrate. Each pillar has a base 164, a central core 172/174, and a top cap 176. The pillars are spaced apart by a distance 166. The device is covered by a top layer 178. The pillars are connected to a horizontal layer 162. The device is also covered by a layer 140. The pillars are connected to a horizontal layer 162. The device is also covered by a layer 140. The pillars are connected to a horizontal layer 162. The device is also covered by a layer 140.

FIG. 30

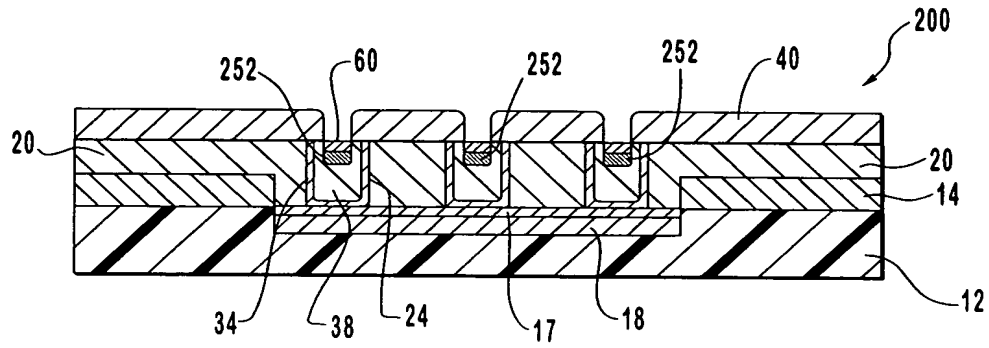


FIG. 31

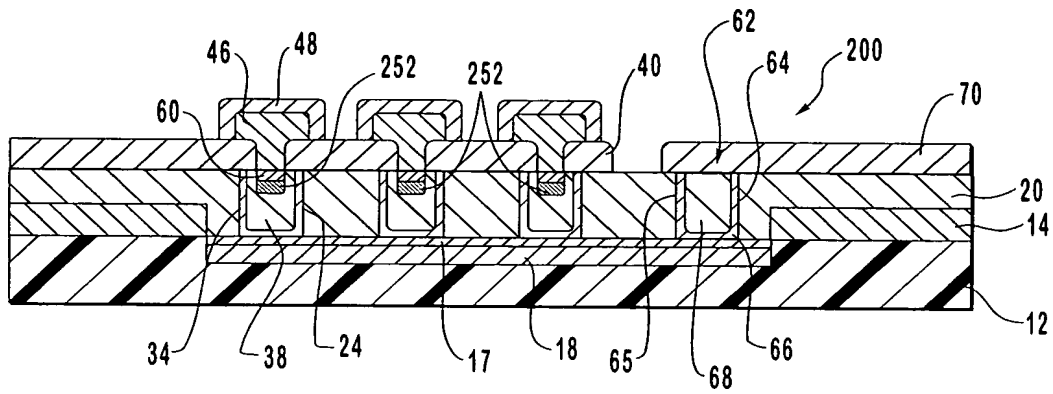


FIG. 32